GE Aviation

Intern/Master Thesis: Interference Channel Analysis (m/f)
Job No. 3221329, Garching

About us
GE Aviation Munich is a R&D center of excellence and is in the heart of southern Germany, on the Garching campus of the Technical University of Munich. This creates a unique blend for our engineers to be in a university setting, while performing research and development in a world-class industrial environment that is dedicated to bringing innovative technologies to market. Within the R&D community, the center maintains close partnerships with numerous universities, research institutions and technology companies in Germany and abroad.

Role Summary
GE Aviation is investigating the use of modern multi-core architectures. You will characterize the interference channels of two different multi-core architectures (NXP T1040 and Xilinx Zynq Ultrascale+). The former is a quad-core Power PC built around the e5500 core, the latter a quad-core ARM built around the A53 core. This can be done either during an internship or for your master thesis.

Essential Responsibilities:

Responsibilities
• Enhance an existing bare-metal test suite
• Develop a test plan
• Characterize interference channels by investigating performance and determinism
• Develop and implement mitigation concepts

Qualifications
• Good C/C++ Skills
• Good understanding of MPSoCs and CPU architectures
• Experience with embedded software development
• Self-motivated, structured work style and good communication skills
• Fluency in English
• Good academic track record

We look forward to receiving your online application!

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